DATA SHEET

OQ2545HP
SDH/SONET STM16/OC48 laser driver

Preliminary specification
File under Integrated Circuits, IC19

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Philips Semiconductors

PHILIPS

FEATURES

- Differential 50 Ω inputs for direct connection to CML (Current-Mode Logic) outputs
- Internal retiming to minimize jitter
- Input clock phase margin of 320° at 2.5 Gbits/s
- RF output current sinking capability of 60 mA for 25 Ω loads and 50 mA for 50 Ω loads
- Bias output current sinking capability of 100 mA
- TTL compatible control inputs
- Loop mode for system testing
- Continuous output monitoring
- Typical power dissipation: 1420 mW
- Low cost LQFP48 plastic package.

APPLICATIONS

- Digital fibre optic modulation driver in STM16/OC48 short, medium and long haul optical transmission systems
- Optical modulation driver in high speed data networks
- High current driver for electro-optical converters
- High current electrical line driver.

GENERAL DESCRIPTION

The OQ2545HP is a driver IC intended to be used with directly modulated laser diodes or with Electro Absorption Modulators (EAMs) in SDH/SONET 2.5 Gbits/s optical transmission systems.

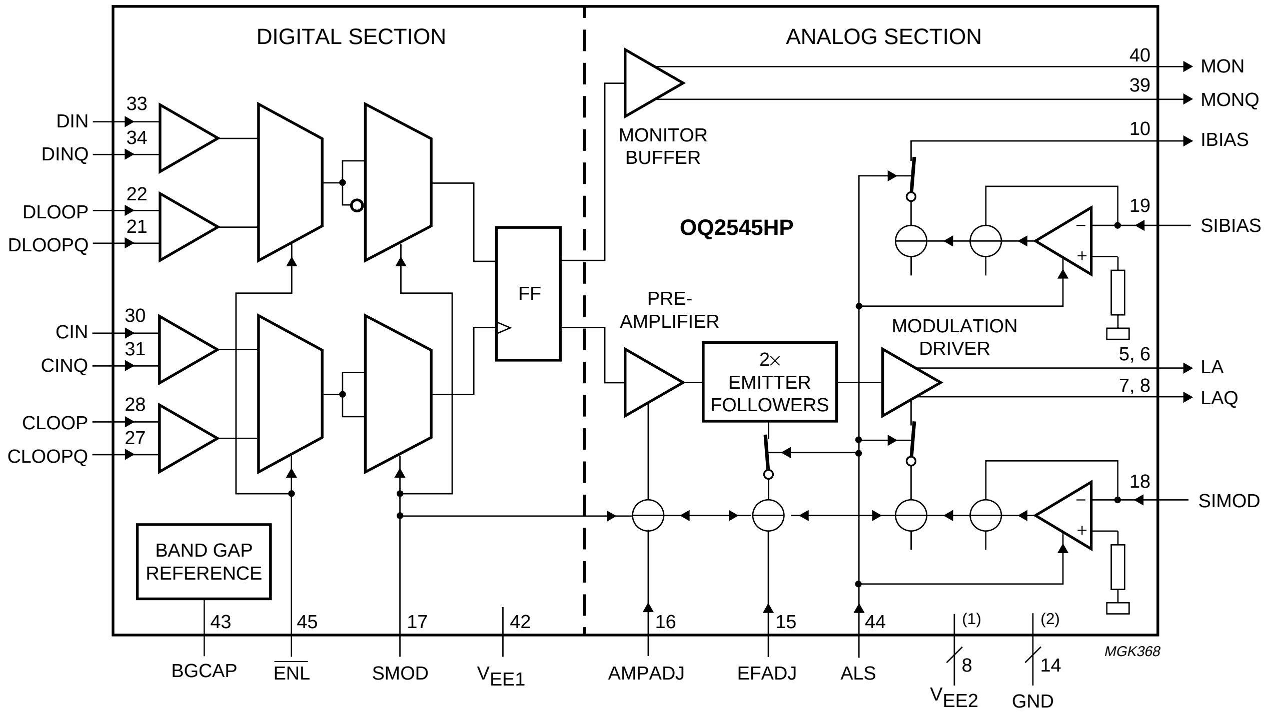
It features differential data and clock inputs and internal retiming for better jitter performance. Loop mode inputs are provided for system testing, along with an output for continuous monitoring.

The high current drive has bias and modulating current outputs, the levels of which can be set separately. As an additional safety measure, the active HIGH ALS (Automatic Laser Shutdown) input can be used to switch off the laser modulation and bias currents. Although the circuit is intended for 2.5 Gbits/s optical transmission systems, it can be used in any application requiring high current drive at high frequencies.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2545HP	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM



(1) Pins 1, 12, 13, 24, 25, 36, 37 and 48

(2) Pins 2, 4, 9, 11, 14, 20, 23, 26, 29, 32, 35, 38, 41 and 47.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE[1]
V_{EE2}	1	supply voltage for analog section	S
GND	2	ground	S
DIOA	3	anode of temperature sensing diode array	A
GND	4	ground	S
LA	5	modulation current output	O
LA	6	modulation current output	O
LAQ	7	modulation current output inverted	O
LAQ	8	modulation current output inverted	O
GND	9	ground	S
IBIAS	10	bias current output	O
GND	11	ground	S
V_{EE2}	12	supply voltage for analog section	S
V_{EE2}	13	supply voltage for analog section	S
GND	14	ground	S
EFADJ	15	input for emitter follower current adjustment	AI
AMPADJ	16	input for preamplifier current adjustment	AI
SMOD	17	data polarity switch	I
SIMOD	18	RF modulated output current adjustment	I
SIBIAS	19	DC output current adjustment	I
GND	20	ground	S
DLOOPQ	21	loop mode data input inverted	I
DLOOP	22	loop mode data input	I
GND	23	ground	S
V_{EE2}	24	supply voltage for analog section	S
V_{EE2}	25	supply voltage for analog section	S
GND	26	ground	S
CLOOPQ	27	loop mode clock input inverted	I
CLOOP	28	loop mode clock input	I
GND	29	ground	S
CIN	30	clock input	I
CINQ	31	clock input inverted	I
GND	32	ground	S
DIN	33	data input	I
DINQ	34	data input inverted	I
GND	35	ground	S
V_{EE2}	36	supply voltage for analog section	S
V_{EE2}	37	supply voltage for analog section	S
GND	38	ground	S
MONQ	39	data monitor output inverted	O
MON	40	data monitor output	O

SYMBOL	PIN	DESCRIPTION	TYPE[1]
GND	41	ground	S
V_{EE1}	42	supply voltage for digital section	S
BGCAP	43	pin for connecting band gap reference decoupling capacitor	A
ALS	44	automatic laser shut down control (active HIGH)	I
$\overline{\text{ENL}}$	45	loop mode enable (active LOW)	I
V_{CC}	46	supply voltage for TTL interface	S
GND	47	ground	S
V_{EE2}	48	supply voltage for analog section	S

Note

1. Pin type abbreviations: O = Output, I = Input, S = power Supply, A = Analog function.

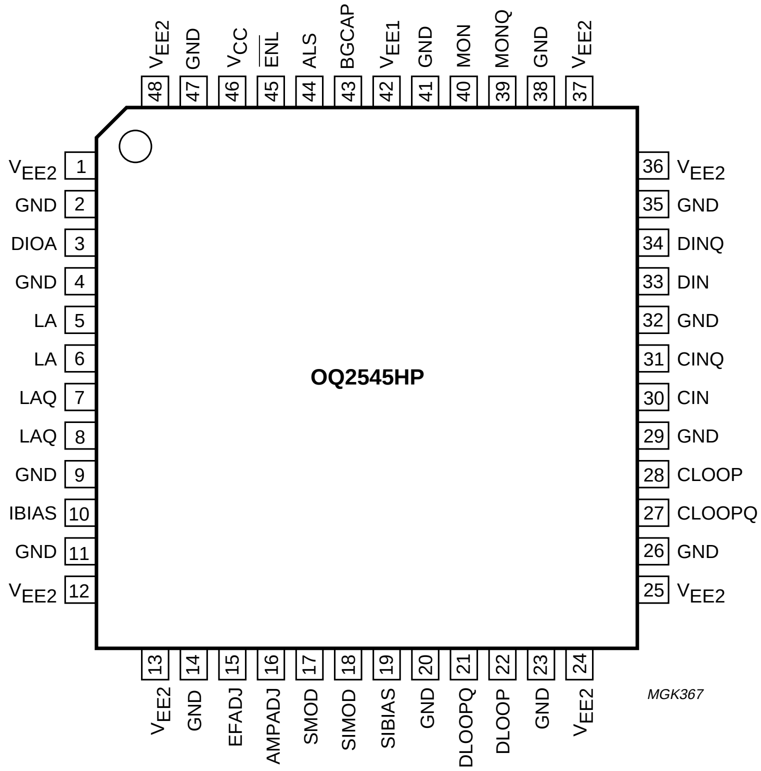


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The OQ2545HP can be divided into two functional blocks:

- A digital section on the input side
- An analog section on the output side.

The input buffers present an impedance of 50 Ω to the data stream on the DIN, DINQ, DLOOP and DLOOPQ differential inputs. The input data is then fed to a multiplexer where normal ($\overline{ENL}$ = HIGH) or loop mode ($\overline{ENL}$ = LOW) inputs are selected. A second multiplexer inverts the input signals when SMOD is connected to V_{EE1} (this is necessary when driving an EAM). An external clock connected to a master-slave flip-flop is then used to retime the data. This reduces jitter on the data signal to a minimum.

The preamplifier following the flip-flop boosts the signal to a suitable level for the modulation driver. Two emitter followers provide the necessary signal isolation between the preamplifier and the high current modulation driver.

The bias currents for the preamplifier and the emitter followers contains an output level dependent component, along with an independent component. The independent component is adjusted by means of the AMPADJ (preamplifier) and EFADJ (emitter followers) inputs. The output level dependent component is controlled by the SIMOD input and the op-amp circuit, which also sets the modulation driver level. The AMPADJ input also controls the shape of the output signal at LA and LAQ.

An independently adjustable on-chip bias current source is provided for when the OQ2545HP is driving directly modulated laser diodes. The SIBIAS input is used to set the bias current level. The output current at IBIAS will be about 106 times greater than the input current at SIBIAS. A similar arrangement is used to control the modulation current at LA and LAQ. The output current at LA and LAQ is approximately 70 times the input current at SIMOD.

The active HIGH TTL compatible ALS input can be used to switch off all current sources. This function makes it possible to implement safety measures that will shut down the circuit in the event of an optical system malfunction.

The buffered differential 50 Ω outputs MON and MONQ can be used to monitor the optically modulated data (at the flip-flop outputs).

Loop mode

Loop mode is provided for system testing. A LOW level on $\overline{ENL}$ selects loop mode. If $\overline{ENL}$ is left open, it is pulled HIGH (TTL) by an internal pull-up resistor.

Automatic laser shutdown

A HIGH level (TTL) on ALS switches off the laser modulation and bias currents. This function allows the circuit to be shut down in the event of an optical system malfunction or for system maintenance. If not connected, ALS is pulled LOW (TTL) by an internal pull-down resistor.

Data monitoring

Pins MON and MONQ can be used as data monitor outputs. They need to be AC-coupled (for example, to a 50 Ω matched RF amplifier with sufficient bandwidth).

Output polarity selection

The SMOD input is used to set the correct logic assignment between data inputs DIN and DINQ (or DLOOP and DLOOPQ) and outputs LA, LAQ, MON and MONQ. This is necessary because directly modulated laser diodes and EAMs have different output voltage requirements. When a laser diode is used, a low voltage on the LA output (and thus a high current because the diode is connected between ground and the LA output) corresponds to a logic HIGH, while a high voltage on the LA output (low current) corresponds to a logic LOW**.**

The opposite is the case with an EAM, so an inversion is needed between input and output. This happens in the second multiplexer (see Fig.1) when SMOD is connected to V_{EE1} (LOW). If left open SMOD is pulled up to GND, which is the laser diode setting.

Modulation current setting

The SIMOD input is used to adjust the modulation current at outputs LA and LAQ. This is achieved by regulating the internal current mirror, which serves as a reference current for the modulation driver. The reference port of the control op-amp is connected to ground through an internal 4 kΩ resistor, thus establishing a ‘virtual earth’ on the SIMOD pin (0 V DC). An external 3 to 4 kΩ resistor connected to an adjustable voltage source is needed to regulate the internal current mirror. This adjustable voltage source could be a part of the laser current control box (see Fig.8). The maximum output current of 60 mA is achieved with a 4 V input. The input current at SIMOD would be about 1 mA in this case.

Bias current setting

An independently adjustable on-chip bias current source is provided for when the OQ2545HP is driving directly modulated laser diodes. The SIBIAS input is used to adjust the bias current at output IBIAS, in a similar arrangement

to that used for adjusting the modulation current.
The reference port of the control op-amp is again connected to ground through an internal 4 kΩ resistor, thus establishing a ‘virtual earth’ on the SIBIAS pin (0 V DC). An adjustable voltage source connected to SIBIAS through a 3 to 4 kΩ resistor is used to regulate the internal current mirror. The maximum output current of 100 mA would be achieved with a 4 V input. The input current at SIBIAS would be about 1 mA in this case.

Band gap decoupling capacitor

The band gap voltage should be decoupled to V_{EE1} with an external 10 nF capacitor to minimize noise. It cannot be used as an external reference voltage for other circuits.

Preamplifier bias current adjustment

The bias current for the preamplifier contains a modulation dependent component and a modulation independent component. The modulation dependent current is adjusted via SIMOD (see Section “Modulation current setting” above). The modulation independent current will be adequate under normal circumstances. However, in some applications it may be necessary to customize the shape of the modulation current. This can be done by adjusting the preamplifier bias current by means of the AMPADJ pin. With this pin left floating, the bias current is 0.6 mA. If this pin is connected to ground, the maximum bias current will be about 3 mA. A resistor can be connected between AMPADJ and ground to adjust the current level within this range. The bias current can be decreased by connecting a resistor between AMPADJ and V_{EE2} (however care should be taken as the preamplifier will not be able to drive the modulation driver if the bias current is too low).

Emitter follower bias current adjustment

The bias currents for the emitter followers connected between the preamplifier and the modulation driver contain two components: a modulation dependent component (controlled via SIMOD; see Section “Modulation current setting” above) and a modulation independent component. The modulation independent currents, 8.2 and 16.4 mA, are sufficient to ensure the emitter followers operate correctly under normal circumstances. In some applications, however, the output currents at LA and LAQ may need to be optimized. This is achieved by connecting an external resistor between the EFADJ pin and ground. If EFADJ is connected directly to ground without using a resistor, the maximum currents for the two emitter followers will be approximately 25 and 50 mA, respectively. Because the emitter followers buffer the signal from the preamplifier, the range over which the current can be adjusted through EFADJ is dependent on the AMPADJ setting.

Grounding and power supply decoupling

The ground connection on the PCB needs to be a large copper area fill connected to a common ground plane with as low inductance as possible. The large area fill will improve heat transfer to the PCB and thus aid IC cooling.

The power supply pins need to be decoupled using chip capacitors mounted as close as possible to the IC.
To avoid high frequency resonance, multiple bypass capacitors should not be mounted at the same location.
To minimise low frequency switching noise in the vicinity of the OQ2545HP, the power supply line should ideally be filtered once using an LC-circuit with a low cut-off frequency.

RF connections

A coupled stripline or microstrip with an odd mode characteristic impedance of 50 Ω (nominal value) should be used for the differential RF connections on the PCB. This applies to the CML differential line pairs CIN and CINQ, DIN and DINQ, CLOOP and CLOOPQ, DLOOP and DLOOPQ and MON and MONQ. In addition, the following lines should not vary in length by more than 10 mm:

- DIN, DINQ, CIN and CINQ
- CLOOP, CLOOPQ, DLOOP and DLOOPQ.

Thermal requirements and cooling

To avoid overheating, the thermal resistance from junction to ambient ($R_{th(j-a)}$) in the vicinity of the package must be less than 25 K/W. The value of $R_{th(j-a)}$ is strongly dependent on the cooling method used and on the layout of the application board. For optimum heat transfer between the die and the PCB, all V_{EE} pins should be connected to large copper area fills. This will normally be effective enough to ensure forced cooling using a heatsink is unnecessary.

ESD protection

In order to achieve high frequency performance, it has been necessary to make adjustments to the standard ESD protection scheme. Inputs DIN, DINQ, CIN, CINQ, DLOOP, DLOOPQ, CLOOP and CLOOPQ and outputs MON and MONQ are protected by a reduced ESD structure and the LA and LAQ outputs have **no protection** against ESD, so extra care should be taken with these pins.

Power consumption

The total power consumption of the OQ2545HP is very much application dependent. Because off the wide range of adjustments that can be made to customize the output for a specific application, only a rough estimate of the total power consumption can be made.

Referring to the block diagram (Fig.1), the blocks in the digital section have a fixed power consumption that is only dependent on process spread and supply voltages. This part of the IC accounts for the terms P_{VEE1} and P_{VCC} in Equation (1) below. The behaviour of the blocks in the analog section can be customized, which means that the total power dissipation in this part of the IC cannot be specified unambiguously.

Whether the IC is being used to drive a laser diode or an EAM has a large impact on the power dissipation level in the analog section. The extra DC quiescent current needed to bias a laser diode means that current consumption will be much greater than when driving an EAM. Apart from this, the settings of the control pins AMPADJ and EFADJ will also influence the power dissipation.

The power dissipation due to AMPADJ and EFADJ can be roughly estimated from the current flowing into these pins. The adjustable internal current in the preamplifier module is about 2 times the external current, so the power dissipated in this module is approximately $3 \times I_{AMPADJ} \times V_{EE2}$ greater than when AMPADJ and EFADJ are left open. In the emitter follower module, the internal current is about 54 times the current into EFADJ, so the power dissipated is approximately $55 \times I_{EFADJ} \times V_{EE2}$ greater than when AMPADJ and EFADJ are left open.

Power consumption due to the laser/EAM modulation current equals $I_{MOD} \times (V_{LA} - |V_{EE2}|)$, where V_{LA} is the minimum voltage at pins LA and LAQ. V_{LA} depends on the external laser/EAM supply voltage and forward voltage drop. V_{LA} can be lowered further by adding additional external resistance as shown in Fig.3. The minimum V_{LA} voltage required for proper operation of the IC can be found in Chapter “Characteristics”. A similar argument is valid for power consumption due to the bias current.

Using the formula in Equation (1) along with the values in Chapter “Application specific power consumption”, it should be possible to estimate the power dissipation for a specific application. The most important constraint on power dissipation is the maximum junction temperature allowed. Under normal circumstances this limits the **maximum power dissipation to <1350 mW**.

$$P_{tot} = P_{VEE1} + P_{VCC} + P_{VEE2} - P_{LA/LAQ} - P_{IBIAS} \quad (1)$$

With careful PCB layout and some means of cooling, it is possible to reduce the thermal resistance from junction to ambient. This opens the possibility of using the OQ2545HP in applications where total power dissipation exceeds 1350 mW. This is illustrated in the graph in Fig.4. If the application specific power dissipation is in the region of the curve where $R_{th(j-a)} \geq 27$ K/W, no extra cooling is required ($P_{tot} < 1350$ mW). If total power dissipation is greater than 1350 mW, cooling will be necessary.

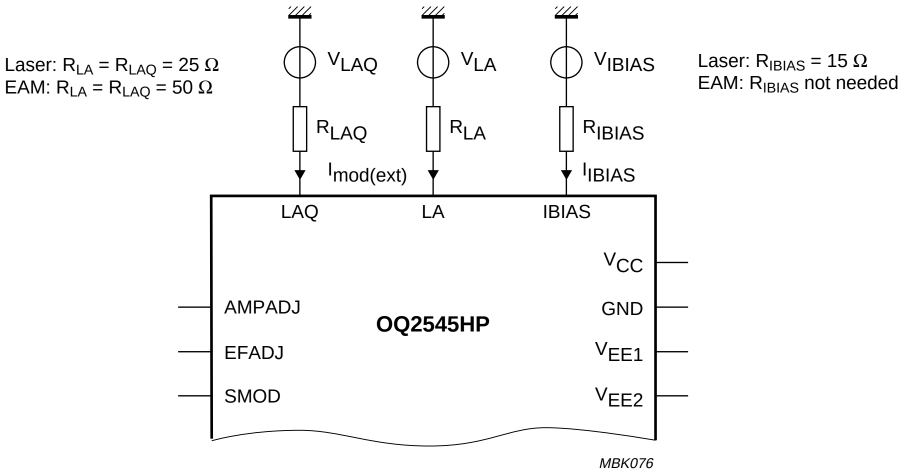


Fig.3 Load dependent power consumption of the OQ2545.

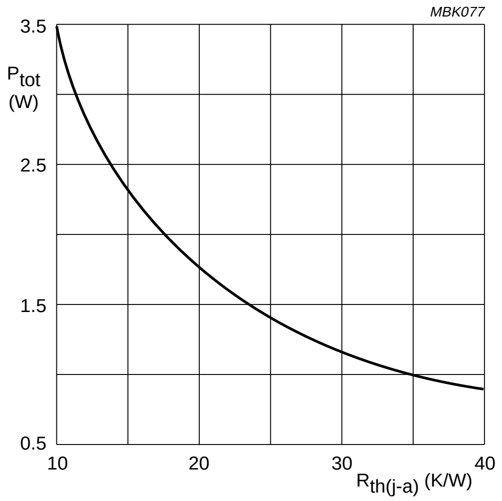


Fig.4 Total power dissipation as a function of thermal resistance.

APPLICATION SPECIFIC POWER CONSUMPTION

V_{EE1} = –4.5 V, V_{EE2} = –6.5 V and V_{CC} = 5 V for typical values; V_{EE1} = –4.75 V, V_{EE2} = –6.85 V and V_{CC} = 5.25 V for worst case values.

SYMBOL	PARAMETER	CONDITIONS	TYP.		WORST CASE		UNIT
			I_{IBIAS} = 0 mA	I_{IBIAS} = 80 mA	I_{IBIAS} = 0 mA	I_{IBIAS} = 80 mA	
Laser diode; note 1							
P_{VEE1}	power consumption at V_{EE1}		315	315	430	430	mW
P_{VCC}	power consumption at V_{CC}		10	10	16	16	mW
P_{VEE2}	power consumption at V_{EE2}	AMPADJ, EFADJ open	975	1500	1300	1800	mW
ΔP_{VEE2}	incremental power consumption at V_{EE2}	AMPADJ connected to GND	40	40	50	50	mW
		EFADJ connected to GND	475	475	500	500	mW
$P_{LA/LAQ}$	power consumption due to modulation current	LA and LAQ terminated with 25 Ω	180	180	180	180	mW
P_{IBIAS}	power consumption due to bias current	IBIAS terminated with 15 Ω	0	100	0	100	mW
P_{tot}	total power dissipation	AMPADJ and EFADJ open circuit	1120	1545	1570	1970	mW
		AMPADJ connected to GND	1160	1585	1620	2020	mW
		EFADJ connected to GND	1595	2020	2070	2470	mW
EAM; note 2							
P_{VEE1}	power consumption at V_{EE1}		310	–	430	–	mW
P_{VCC}	power consumption at V_{CC}		10	–	16	–	mW
P_{VEE2}	power consumption at V_{EE2}	AMPADJ and EFADJ open circuit	1070	–	1370	–	mW
ΔP_{VEE2}	incremental power consumption at V_{EE2}	AMPADJ connected to GND	40	–	50	–	mW
		EFADJ connected to GND	465	–	500	–	mW
$P_{LA/LAQ}$	power consumption due to modulation current	LA and LAQ terminated with 25 Ω	125	–	125	–	mW
P_{IBIAS}	power consumption due to bias current	IBIAS terminated with 15 Ω	0	–	0	–	mW
P_{tot}	total power dissipation	AMPADJ and EFADJ open circuit	1265	–	1700	–	mW
		AMPADJ connected to GND	1305	–	1750	–	mW
		EFADJ connected to GND	1730	–	2200	–	mW

Notes

1. With reference to Fig.3:
   a) I_{IBIAS} = 0 or 80 mA.
   b) $I_{mod(ext)}$ = 60 mA ($I_{mod(int)}$ = 75 mA).
   c) R_{LA} = R_{LAQ} = 25 Ω; R_{IBIAS} = 15 Ω.
   d) V_{LA} = V_{LAQ} = V_{IBIAS} = –1.5 V.
2. With reference to Fig.3:
   a) I_{IBIAS} = 0 mA (left open circuit).
   b) $I_{mod(ext)}$ = 50 mA ($I_{mod(int)}$ = 75 mA).
   c) R_{LA} = R_{LAQ} = 50 Ω.
   d) V_{LA} = V_{LAQ} = 0 V.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage for TTL interface	–0.5	+6.0	V
V_{EE1}	supply voltage for digital interface	–6.0	+0.5	V
V_{EE2}	supply voltage for analog interface	–7.5	+0.5	V
V_n	DC voltage			
	pins 21, 22, 27, 28, 30, 31, 33, 34, 39 and 40	–1.0	+0.5	V
	pins 44 and 45	–0.5	V_{CC} + 0.5	V
	pins 15, 16, 18 and 19	V_{EE2} – 0.5	+0.5	V
	pins 17 and 43	V_{EE1} – 0.5	+0.5	V
I_n	DC input current			
	pins 5, 6, 7 and 8	–	80	mA
	pin 10	–	110	mA
	pin 3	–	10	mA
P_{tot}	total power dissipation	–	1350(1)	mW
T_j	junction temperature	–	150	°C
T_{stg}	storage temperature	–65	+150	°C

Note

1. The value specified for total power dissipation is the maximum allowed for an LQFP48 package without forced cooling. See Section “Power consumption” for details of application specific power dissipation.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point	27	K/W

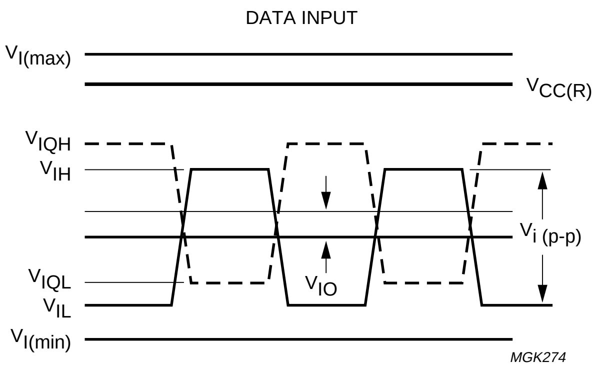


Fig.5 Logic level symbol definitions for CML inputs.

CHARACTERISTICS

At nominal supply voltages; T_{amb} = 25 °C; 50 Ω loads on OUT and OUTQ.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{CC}	supply voltage for TTL interface		4.75	5.0	5.25	V
V_{EE1}	supply voltage for digital interface		–4.75	–4.5	–4.25	V
V_{EE2}	supply voltage for analog interface		–6.85	–6.5	–6.15	V
I_{CC}	supply current for TTL interface		–	2	3	mA
I_{EE1}	supply current for digital interface		–	70	90	mA
I_{EE2}	supply current for analog interface					
	with EAM	note 1	–	165	200	mA
	with laser diode	note 1	–	150	180	mA
	for ALS		–	5	7	mA
P	power dissipation					
	laser diode application	note 2	–	1120	1570	mW
	laser diode application	note 3	–	1545	1970	mW
	EAM application	note 4	–	1265	1700	mW
	during ALS		–	350	380	mW
T_{amb}	ambient temperature		–40	–	+85	°C
T_j	junction temperature		–	–	+125	°C
CML data and clock inputs: DIN, DINQ, CIN, CINQ, DLOOP, DLOOPQ, CLOOP and CLOOPQ; note 5						
$V_{i(p-p)}$	input voltage (peak-to-peak value)		100	250	500	mV
V_{IO}	permitted input offset voltage		–25	0	+25	mV
$V_{I,IQ}$	input voltages		–600	–200	+250	mV
Z_i	single ended input impedance		40	50	60	Ω
TTL input: $\overline{\text{ENL}}$; note 6						
V_{IL}	LOW-level input voltage		–	0.4	0.8	V
V_{IH}	HIGH-level input voltage		2.4	4.0	–	V
I_{IL}	LOW-level input current		–380	–	0	µA
I_{IH}	HIGH-level input current		0	–	210	µA
TTL input: ALS; note 6						
V_{IL}	LOW-level input voltage		–	0.4	0.8	V
V_{IH}	HIGH-level input voltage		2.4	4.0	–	V
I_{IL}	LOW-level input current		–90	–	0	µA
I_{IH}	HIGH-level input current		0	–	500	µA
t_{res}	ALS response time	note 7	–	–	1.5	ms
Current source control inputs: SIMOD and SIBIAS; voltage controlled with 39 kΩ source resistance; note 8						
B	unity gain bandwidth	note 9	–	10	–	MHz
ΔG	gain peaking	note 10	–	1	6	dB
SR	slew rate		–	4	–	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Amplifier adjustment: AMPADJ						
$I_{I(AMPADJ)}$	preamplifier control current		–	–	1	mA
Emitter follower adjustment: EFADJ						
$I_{I(EFADJ)}$	control current for emitter followers		–	–	1	mA
Band gap voltage: BGCAP						
V_{BGCAP}	band gap voltage	note 11	–2.03	–1.6	–1.35	V
Temperature diodes: DIOA						
$\Delta V_{DIOA-VEE2}$	temperature dependent output voltage;	$I_{I(d)}$ = 1 mA; note 12	1.7	2.07	2.5	V
Laser modulation outputs: LA and LAQ; note 13						
I_{OL}	LOW-level output current	laser diode; LAQ terminated with 25 Ω	5	–	60	mA
I_{OH}	HIGH-level output current		–	–	1	mA
$I_{O(ALS)}$	output current during ALS		–	–	1	mA
V_O	output voltage		–3.5	–	0	V
δ	duty factor; note 14	laser diode; RF load impedance of 25 Ω on both terminals	45	50	55	%
t_r	rise time; note 15		–	110	150	ps
t_f	fall time; note 15		–	140	150	ps
$J_{o(p-p)}$	output jitter (peak-to-peak value)		–	20	40	ps
I_{OL}	LOW-level output current	EAM; LAQ terminated with 50 Ω	25	–	50	mA
I_{OH}	HIGH-level output current		–	–	1	mA
$I_{O(ALS)}$	output current during ALS		–	–	1	mA
V_O	output voltage		–3.5	–	0	V
δ	duty factor; note 14	EAM; RF load impedance of 50 Ω on both terminals	45	50	55	%
t_r	rise time; note 15		–	140	200	ps
t_f	fall time; note 15		–	175	200	ps
$J_{o(p-p)}$	output jitter (peak-to-peak value)		–	15	40	ps
Z_o	single ended output impedance	LAQ terminated with 50 Ω	80	100	120	Ω
BR	bit rate		–	2.5	3.0	Gbits/s
Bias current output: IBIAS; note 16						
I_O	output current		1	–	100	mA
$I_{O(ALS)}$	output current during ALS		–	–	1	mA
V_O	output voltage	note 17	V_{EE1} + 0.6	–	0	V
V_{LASER}	laser voltage drop		1.0	1.3	1.6	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Monitor outputs: MON and MONQ						
$V_{o(p-p)}$	signal voltage swing		100	150	250	mV
V_O	DC output voltage		–1.85	–	–1.35	V
Z_o	single ended output impedance		40	50	60	Ω
δ	duty factor	note 14	48	50	52	%
t_r	rise time	note 15	–	100	150	ps
t_f	fall time	note 15	–	100	150	ps
$J_{o(p-p)}$	output jitter (peak-to-peak value)		–	10	40	ps
Clock phase margin						
$T_{cy(CIN)}$	input clock period		–	402	–	ps
t_{su}	set-up time		100	20	–	ps
t_h	hold time		100	20	–	ps
φ_m	clock phase margin		180	320	335	deg

Notes

1. Values are based on an internal modulation current of 75 mA, without a bias source (I_{IBIAS} = 0 mA). See Section “Power consumption” for further details on application specific power dissipation. AMPADJ and EFADJ are left open circuit.
2. For I_{IBIAS} = 0 mA; LA and LAQ both terminated with 25 Ω; total modulation current of 75 mA.
   Due to the internal 100 Ω collector resistors at the LA and LAQ outputs, part of the modulation current will be drawn from the IC’s own supply and will not be available through the LA and LAQ pins. The ratio of available to total modulation current is 100 : 100 + R_{ext} ($R_{ext} = R_{LA} = R_{LAQ}$). Therefore, with R_{ext} = 25 Ω, the available modulation current equals 60 mA$\left(\frac{100}{125} \times 75\right)$. See Section “Power consumption” for further details. AMPADJ and EFADJ are left open circuit.
3. For I_{IBIAS} = 80 mA; LA and LAQ both terminated with 25 Ω; total modulation current of 75 mA. Detailed information can be found in Section “Power consumption”. AMPADJ and EFADJ are left open circuit.
4. For I_{IBIAS} = 0 mA; LA and LAQ both terminated with 50 Ω; total modulation current of 75 mA.
   Due to the internal 100 Ω collector resistors at the LA and LAQ outputs, part of the modulation current will be drawn from the IC’s own supply and will not be available through the LA and LAQ pins. The ratio of available to total modulation current is 100 : 100 + R_{ext} ($R_{ext} = R_{LA} = R_{LAQ}$). Therefore, with R_{ext} = 50 Ω, the available modulation current equals 50 mA$\left(\frac{100}{150} \times 75\right)$. See Section “Power consumption” for further details. AMPADJ and EFADJ are left open circuit.
5. See Fig.5 for CML symbol definitions. All CML inputs are terminated internally using 50 Ω on-chip resistors to GND.
6. Since the TTL inputs are static, no timing specifications are given in this data sheet.
7. The response time is the time it takes the laser currents (I_{LA} and I_{IBIAS}) to fall to below 1 mA after a logic HIGH has been applied to pin ALS.
8. The values given in the table are valid for capacitive loads of up to 50 pF connected to these input pins.
9. The current converters consist of op-amps used as unity gain amplifiers and current mirrors. The specified characteristics apply for the transfer function from SIMOD to LA and LAQ or from SIBIAS to IBIAS.
10. Although the op-amps are configured as unity gain amplifiers, the response tends to peak close to the roll-off area.

11. To suppress supply noise in the band gap, an external capacitor of 10 nF may be connected between this pin and V_{EE1}.
12. Three series-connected diodes have been integrated for measuring junction temperature. The anode of the diode array is connected to DIOA. The cathode is connected internally to V_{EE2}. With a current of 1 mA, the anode voltage (measured with reference to V_{EE2}) will be somewhere within the specified range, depending on temperature. This voltage will show a –6 mV/°C gradient over temperature.
13. The currents flowing into LA and LAQ are not equal to the internal RF modulation current because of an additional current in the internal termination resistors.AMPADJ and EFADJ are left open circuit for all measurements.
14. Duty factor is defined as $\frac{t_H}{T_{cy}} \times 100\%$
15. Rise and fall times are between 10 and 90% of peak values.
16. The DC current into IBIAS is not equal to the internal DC current because of an additional current from the internal termination resistors.
17. To avoid saturation of the IBIAS current source, the voltage level at the IBIAS output should never be allowed to fall below the specified minimum.

TIMING

Input timing

Set-up and hold time definitions are illustrated in Fig.6. The timing characteristics are applicable in both normal and loop modes.

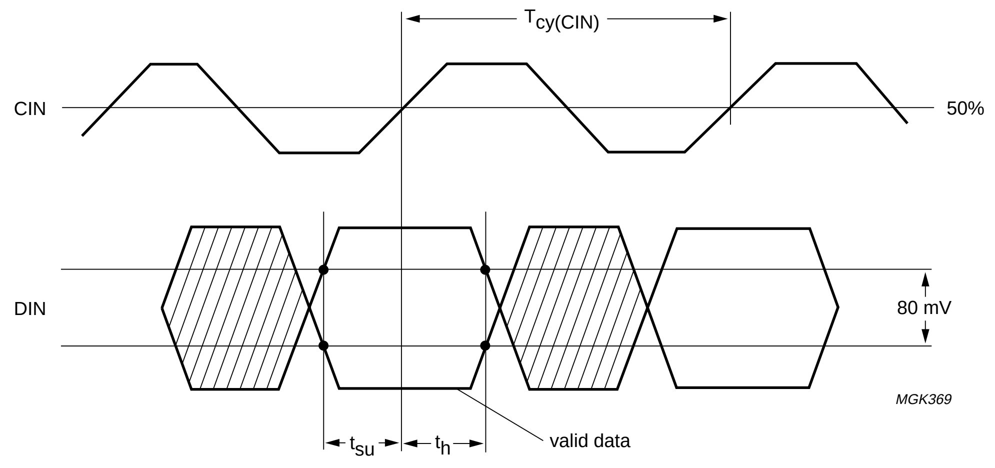


Fig.6 CML input timing.

Output timing

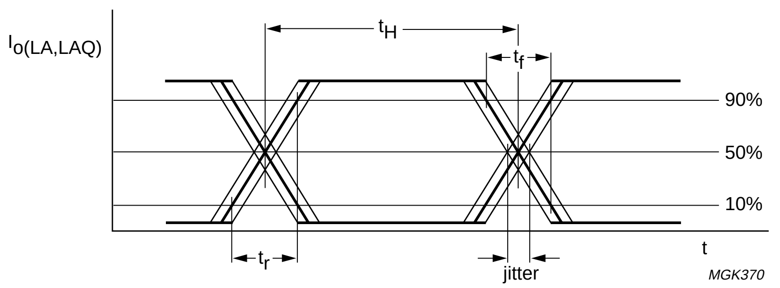
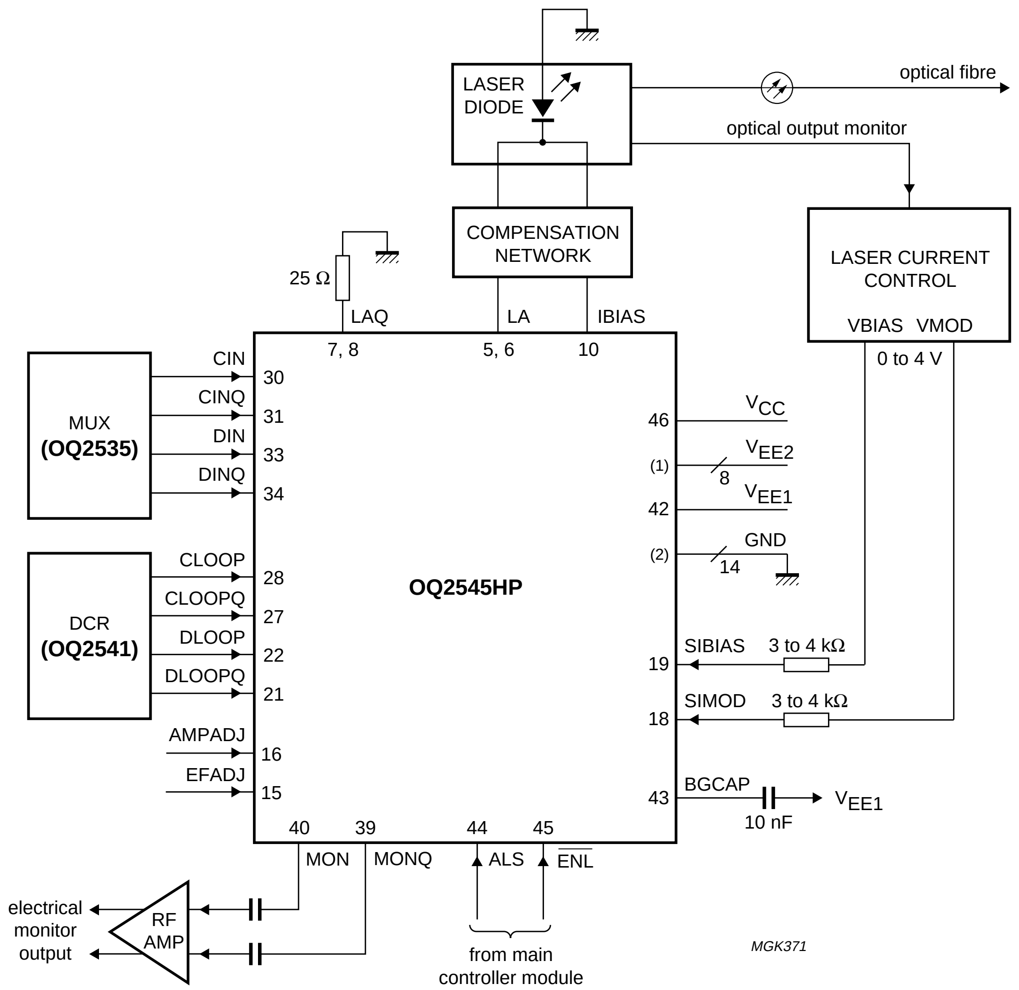


Fig.7 TTL outputs.

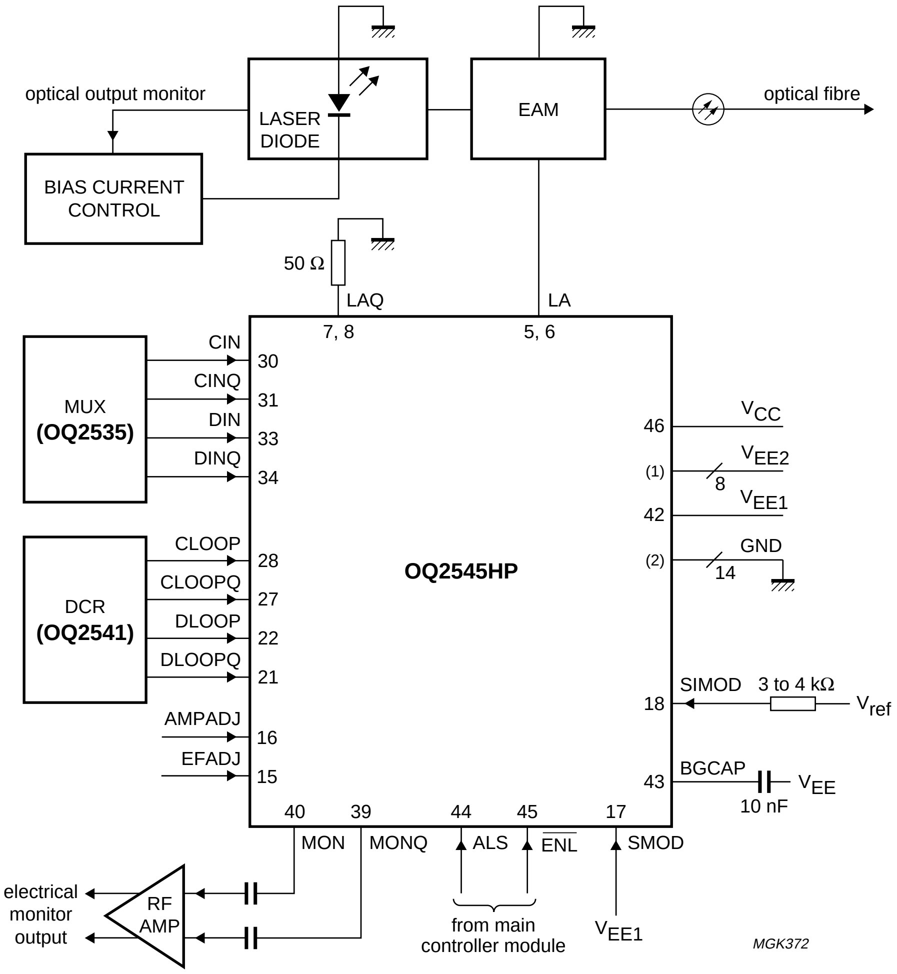
APPLICATION INFORMATION



(1) V_{EE2} pins (pins 1, 12, 13, 24, 25, 36, 37 and 48) should be connected together.

(2) All GND pins (pins 2, 4, 9, 11, 14, 20, 23, 26, 29, 32, 35, 38, 41 and 47) must be connected directly to the PCB ground plane.

Fig.8 Application schematic with laser diode.



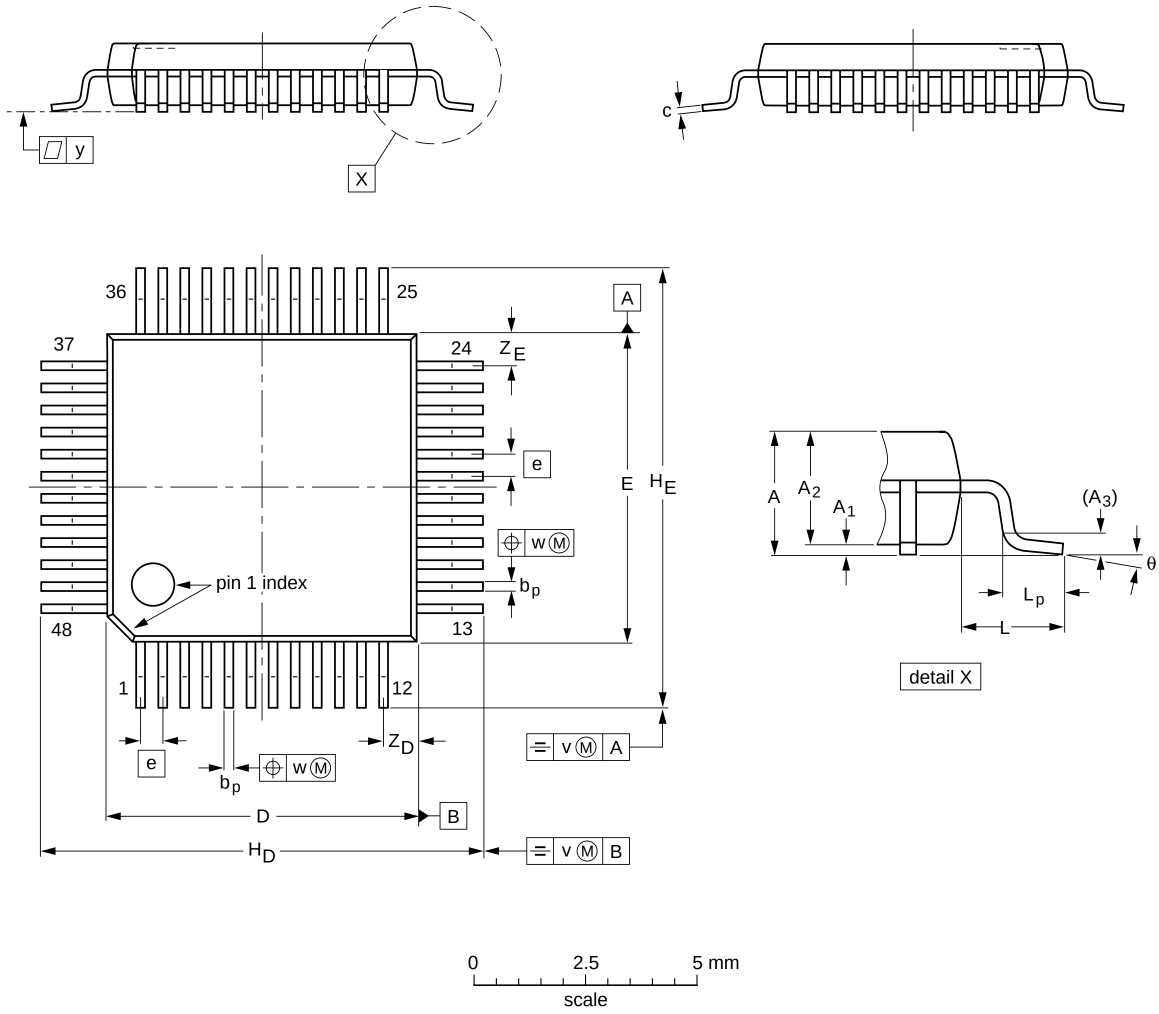
(1) V_{EE2} pins (pins 1, 12, 13, 24, 25, 36, 37 and 48) should be connected together.

(2) All GND pins (pins 2, 4, 9, 11, 14, 20, 23, 26, 29, 32, 35, 38, 41 and 47) must be connected directly to the PCB ground plane.

Fig.9 Application schematic with electro absorption modulator.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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